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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,608	02/19/2004	Vincent Hool	ALTRP099/A1197	1575

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EXAMINER	
CHAMBLISS, ALONZO	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,608	HOOL ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-18 and 20-28* is/are rejected.

7)☒ Claim(s) *11 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The previous restriction requirement mailed on 1/26/06 has been withdrawn. Claims 1-28 are currently pending in the application.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 2/19/04 was filed before the mailing date of the non-final rejection on 5/10/06. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. The formal drawings filed on 2/19/04 have been approved by the examiner.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: " METHOD OF DESIGNING A MODULATED FLIP CHIP SUBSTRATE DESIGN ".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 7, 9, 10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tain et al. (US 6,319,752).

With respect to Claims 1, 4, 9, 10, 12, and 13, Tain teaches receiving a report (i.e. netlist) identifying end connection points for the plurality of electrical paths and identifying a set of coordinates that correspond to a set of I/O pad locations on the die, the set of coordinates being relative to the die, the plurality of electrical paths including signal, power, and ground electrical paths. Dividing the plurality of electrical paths into sections including a first end section (i.e. bumps 302), an intermediate section (i.e. rat connections that are the solid lines between 302 and 402), and a second end section (i.e. pins 402). Cells are selected for the first end section (i.e. array of bumps 302) and the second end section (i.e. array of pins 402). The cells (i.e. the array 302 and 402) represent a first end cell and a second end cell, wherein the first end cell comprises a plurality of first end electrical paths defined by a common constraint. The common constraint is an electrical predefined parameter which has an inherent polarity (i.e. state of being positive or negative). Each first end electrical path includes one of the end connection points that corresponds to the set of coordinates. Connecting the first end cell to the second end cell with transmission lines (i.e. rat connections) to form the plurality of electrical paths. The transmission lines correspond to the intermediate section (see col. 1 lines 10-50 and col. 3 lines 20-67, claims 1-5; Figs. 1-6).

With respect to Claim 2, Tain teaches wherein the report identifies which end connection points are going to be interconnected (col. 3 lines 35-45).

With respect to Claim 3, Tain teaches wherein the report also identifies a set of coordinates that corresponds to a set of I/O pad locations on the die 300 (see col. 1 lines 25-37 and col. 3 lines 35-45).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tain et al. (US 6,319,752) as applied to claim 1 above, and further in view of Chou et al. (US 5,691,568).

With respect to Claims 5 and 6, Tain fails to disclose a substrate wherein the first and second end sections include a portion of at least one electrical path that traverses the plurality of layers and an intermediate section includes a portion of at least one electrical path that traverses only one of the plurality of layers. However, Chou discloses a substrate wherein the first and second end sections include a portion of at least one electrical path 216b, 216d (i.e. vias) that traverses the plurality of layers 206a-206c and an intermediate section 216c (i.e. vias) includes a portion of at least one electrical path that traverses only one of the plurality of layers 206a-206c (col. 3 lines 5-67 and col. 4 lines 1-55; Figs. 2A, 2B, 3, and 4). Thus, Tain and Chou have substantially the same environment of a substrate with chip mounted on the first surface and external connectors on the second surface. Therefore, one skilled in the art would readily recognize incorporating vias with the traces (i.e. rat connections) of Tain, since the vias would provide the intermediate electrical connections the chip and an external device as taught by Chou.

9. Claims 8, 14-18, and 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tain et al. (US 6,319,752) as applied to claim 1 above, and further in view of Kida et al. (US 5,877,942).

With respect to Claim 8, Tain fails to disclose automatically aligning the first end cell, transmission lines, and second end cell such that the first end, intermediate, and second end electrical paths form the electrical paths with corresponding end connection points that are consistent with the report. However, Kida discloses automatically aligning (i.e. to prevent short circuiting or interference by crossing electrical paths) the

first end cell, transmission lines, and second end cell such that the first end, intermediate, and second end electrical paths form the electrical paths with corresponding end connection points that are consistent with the report (see col. 3 lines 1-48). Thus, Tain and Kida have substantially the same environment of a netlist utilized to determined the electrical path trace and vias in a substrate. Therefore, one skilled in the art would readily recognize incorporating an automatically aligning process in the netlist of Tain, since the automatically aligning process would improve the electrical path for substrate while reducing the production cost as taught by Kida

With respect to Claims 14 and 15, Kida discloses the common constraint comprises a geometrical parameter that includes electrical path spacing and electrical path thickness (see col. 2 lines 45-60).

With respect to Claim 16, Tain discloses the common constraint comprising a set ratio (i.e. number) of signal, power, or ground electrical paths amongst the plurality of first end electrical paths (see col. 1 lines 10-50).

With respect to Claims 17 and 24, Tain discloses wherein the second end cell (i.e. pins 402) comprises a plurality of second end electrical paths defined by a second common constraint (i.e. signal) , wherein each second end electrical path includes one of the end connection points that inherently has a BGA coordinate relative to the set of coordinates (see col. 3 lines 25-67; Figs. 1 and 4-6).

With respect to Claims 18, 20, and 21, Tain discloses a second common that is an electrical predefined parameter, which has an inherent polarity (i.e. state of being positive or negative) (see col. 1 lines 25-50).

With respect to Claims 22 and 23, Kida a second common constraint (i.e. for the terminal pads on the bottom of the substrate) comprises a geometrical parameter that is selected from the group consisting of electrical path spacing and electrical path thickness (see col. 2 lines 39-67).

With respect to Claims 25-28, Kida discloses the transmission lines (i.e. traces and vias) comprise a plurality of intermediate electrical paths defined by a third common constraint, wherein each intermediate electrical path is further defined by corresponding first end and second end electrical path. The third common constraint is predefined based on the geometrical parameter that is for electrical path spacing (see col. 2 lines 39-67).

Allowable Subject Matter

10. Claims 11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reason for the indication of allowance subject matter: the prior art of record does not teach or suggest the combination a common constraint that is selected based on one of the plurality of first end electrical paths having the greatest limitation on the common constraint in claims 11 and 19

The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

11. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/May 10, 2006